# Session 6 Overview

# UWB Transceivers

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The resurgence of the telecommunication industry is again reflected by the plethora of wireless data communication devices on offer from the conference's technical program. Of particular note is the continued rise of UWB wireless transceivers, devices that promise half a gigabit per second (or more) of data rate in and out of computers, printers, and home entertainment appliances at short distances. UWB transceivers turn out to present stiff technical challenges and a variety of solutions are presented in this session, that scale the obstacles from different angles.

RF transceivers based on the multi-band OFDM alliance (MBOA) standard continue to make a strong showing this year; with receiver, synthesizer, and transceivers realized in increasing levels of sophistication and CMOS technologies ranging from 90nm to 0.18µm in feature size. The sophistication and integration level are reflected in terms of compliance to WiMedia standard, inclusion of digital PHY on the same chip, or antenna diversity using phased-array techniques. This suggests that UWB is growing into a commercially viable system. A notable trend is that pulse-based or carrier-less UWB receiver and transceiver are making their presence felt this year at the Conference.

Pulse-based UWB systems are addressed in the first two papers of this session. In Paper 6.1, the emphasis is on low power consumption where a 20Mpulses/s receiver is presented that draws an overall current of 16mA from a 1.8V supply. In Paper 6.2, a carrier-less impulse-based transceiver chipset is introduced. It features a measured data-communication rate of up to 200Mb/s while the transmitter can potentially achieve data rates up to 400Mb/s.

In Paper 6.3, antenna diversity and integrated RF selectivity are combined in a 0.18µm CMOS phased-array transceiver. The transmitter achieves an EVM of -27.2dB for 480Mb/s with an FCC mask-compliant output spectrum without any external bandpass filters.

A 90nm CMOS UWB transceiver, powered from a 1.1V supply, is described in Paper 6.4. The chip includes a 12-band synthesizer and covers the frequencies from 3.1 to 9.5GHz.

A full transceiver that fulfills WiMedia/MBOA requirements is presented in Paper 6.5. It has a noise figure in the range of 3.6 to 4.1dB for bands 1 to 3 and a transmitter $P_{1dB}$ of +5dBm at maximal gain.

The integration goes even further in Paper 6.6 where a fully integrated UWB PHY in 0.13µm CMOS is presented. The chip supports both fixed and frequency-hopped modes in the 3.1 to 4.8GHz bands and achieves measured data rates of up-to 480Mb/s.

The last two presentations focus on important building blocks for UWB applications. Paper 6.7 presents a frequency synthesizer that covers the full 14 bands and is realized in 0.18µm CMOS. Finally, a receiver front-end consisting of the LNA, mixer, and IF bandpass filter is presented in Paper 6.8. It is realized without any on-chip or off-chip inductors, and therefore, occupies an active area of 0.35mm$^2$.

 

**6.1 A 16mA UWB 3-to-5GHz 20MPulses/s Quadrature Analog Correlation Receiver in 0.18µm CMOS** **1:30 PM**

*J. Ryckaert,* IMEC, Leuven, Belgium

A 3-to-5GHz quadrature analog correlation RX for UWB impulse radio draws 16mA at 20MPulses/s, making it suitable for low-power low-data-rate applications. The RX is fully integrated in a CMOS 0.18µm process and comprises an LNA, quadrature LO generation and mixers, baseband filtering, an integrator, timing circuitry, and an ADC.

**6.2 A CMOS Carrier-less UWB Transceiver for WPAN Applications** **2:00 PM**

*Y. Zheng,* Institute of Microelectronics, Singapore, Singapore

A carrier-less impulse-based UWB transceiver (TRX) chipset is presented. The TRX employs high-order pulse transmission with analog pulse-position modulation. Realized in a 0.18µm CMOS process, the TRX achieves a NF in the range of 7.7 to 8.1dB, an IIP3 of -12.3dBm, and a sensitivity of -80 to -72dBm. It consumes 76mW and 81mW from a 1.8V supply in transmit and receive modes, respectively.

**6.3 A Dual-Antenna Phased-Array UWB Transceiver in 0.18µm CMOS** **2:30 PM**

*S. Lo,* Tzero Technologies, Sunnyvale, CA

A dual-antenna UWB transceiver in 0.18µm CMOS for mode 1 OFDM applications employs the techniques of antenna diversity and integrated RF selectivity. The packaged device achieves an overall NF of 4.7dB, an IIP3 of -0.8dBm, a TX P1dB of 3.1dBm, and an EVM of -27.2dB for 480Mb/s. The transmit output spectrum is fully compliant with FCC mask for UWB without any external BPF.

**6.4 A 1.1V 3.1-to-9.5GHz MB-OFDM UWB Transceiver in 90nm CMOS** **3:15 PM**

*A. Tanaka,* NEC, Sagamihara, Japan

A 3.1-to-9.5GHz UWB transceiver is implemented in 90nm CMOS technology. It includes a 12-band synthesizer and wideband TX/RX chains operating from a 1.1V supply. The transceiver provides a TX OIP3 of 7.2 to 8.6dBm, an RX gain of 58 to 64dB, and a NF of 6.3 to 7.8dB across 12 bands.

**6.5 A WiMedia/MBOA-Compliant CMOS RF Transceiver for UWB** **3:45 PM**

*M. Tiebout,* Infineon, Munich, Germany

A fully integrated WiMedia/MBOA-compliant RF transceiver for UWB data communication in the 3 to 5GHz band is presented. It is designed in a 0.13µm standard CMOS process with 1.5V single supply voltage. The NF is between 3.6 and 4.1dB over all 3 bands. On the TX side, the $P_{1dB}$ is 5dBm supporting an EVM of -28dB and up to -4dBm output power. A single-PLL LO generation is included.

**6.6 A Fully Integrated UWB PHY in 0.13µm CMOS** **4:15 PM**

*T. Aytur,* Realtek, Irvine, CA

A direct-conversion RF transceiver and digital PHY are integrated in a single 0.13µm digital CMOS chip. Designed for UWB OFDM operation as proposed by the WiMedia Alliance, the device supports both fixed and frequency-hopped modes in the band of 3.1 to 4.8GHz. The RF transceiver draws 100mA in receive mode and 70mA in transmit mode, and the complete chip occupies 17mm$^2$.

**6.7 A 14-band Frequency Synthesizer for MB-OFDM UWB Application** **4:45 PM**

*C-F. Liang,* National Taiwan University, Taipei, Taiwan

A 14-band frequency synthesizer for UWB application is realized in a 0.18µm CMOS process. It uses two PLLs and three mixers. The unwanted spurs due to frequency mixing are at least 35dB lower than the output carriers by using a quadrature divide-by-3 circuit and a 2-stage single-sideband mixer. The core circuit area is 1.5mm$^2$ and the power consumption is 160mW.

**6.8 A sub-1mm$^2$ Dynamically Tuned CMOS MB-OFDM 3-to-8GHz UWB Receiver Front-End** **5:00 PM**

*M. Ranjan,* University of California, San Diego, CA

A 3-to-8GHz heterodyne receiver front end for MB-OFDM UWB systems consisting of an LNA, a mixer, and an on-chip IF BPF is presented. Designed in 0.18µm CMOS, it uses no on-chip inductors or any off-chip components. Measured NF is 5.5dB, IIP2 is 33dBm, and the chip draws 19.5mA from a 2.3V supply.